REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 3, 4, 6-8, 11, 12 and 18-20 are presently pending in this application, Claim 1 having been amended and Claims 19 and 20 having been newly added by the present amendment.

In the outstanding Office Action, Claim 1 was objected for informality; Claims 1-4 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sakamoto et al. (U.S. Patent 6,687,985) in view of Jones et al. (U.S. Patent 5,541,450); and Claims 6 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sakamoto et al. in view of Jones et al. and Londa (U.S. Patent 5,963,430).

Claim 1 has been amended to correct the noted informality in response to the objection, and Claims 19 and 20 have been added herein. These additions in the claims find support in the specification, claims and/or drawings as originally filed, for example, Figure 2, and no new matter is believed to be added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Briefly recapitulating, Claim 1 is directed to a multi-layer printed wiring board and recites: "a first substrate having an opening and having a plurality of external terminals positioned to be connected to a package substrate; a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board, the second substrate having a metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the metallic layer portion; and an IC component having a plurality of terminals and loaded in the opening of the first substrate such that the terminals of the IC component face an opposite

side of the metallic layer portion of the second substrate, wherein the IC component is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC component."

By providing such a second substrate, heat generated by the IC component is effectively radiated to and removed through the metallic layer portion and the non-through holes connected to the metallic layer portion in the second substrate, thereby preventing heat damage caused by the IC component.

The Office Action states that "Sakamoto et al. discloses a multi-layer printed wiring board as shown in figure 1 comprising ... a second substrate (11a, 12) laminated to the first substrate (12, 11b) having a plurality of terminals ... and having a metallic layer portion (electrodes 22) positioned in the opening (15) of the first substrate (12, 11b), and a plurality of non-through holes (see figure 1) filled with conductive materials (14) and electrically connected to the metallic layer (22), a carrier board (16) having terminals (21) formed in the opening and connected to the metallic layer (22) of the second substrate (11a)" but "Sakamoto does not specific [*sic*] disclose an IC formed in the opening having terminals opposite side of the metallic layer such that the metallic layer and non-through holes of the second substrate being [*sic*] irradiate heat generated by the IC component." The Office Action concludes that because "Jones shows a BGA semiconductor package (30) as shown in figure 2 comprising a first substrate (31) having an opening (33) loaded with an IC (18) having terminals (22) formed on top surface of the IC (18), the IC (18) formed on a metallic layer portion ...," "[i]t would have been obvious ... to have a teaching of Jones employed in the wiring board of Sakamoto et al. in order to form a multi-electronic/chip package."

However, it is respectfully submitted that Sakamoto et al. and Jones et al. do not teach or suggest "a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board, the second substrate having

a metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the metallic layer portion ..., wherein the IC component is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC component" as recited in amended Claim 1.

As discussed in the previous response, Sakamoto et al. simply shows a structure in which a carrier board 16 is set in a cavity 15 of a mother board 11 and electrically connected to the mother board 11, and electrodes 22 are connected to carrier board electrodes when the carrier board 16 is set in the mother board 11. Furthermore, according to the Sakamoto et al., via-hole conductors 14 are formed in the substrates 12 and simply provide electrical connection between mother-board-wiring-layers.[1] As such, Sakamoto et al. clearly fails to disclose a substrate having a metallic layer and non-through holes connected to the metallic layer which are structured in a manner that heat generated by an IC chip accommodated in an opening of another substrate is irradiated.

Jones et al. shows a perimeter BGA package or structure 30 in which a semiconductor die 18 is set in an opening 33 of a substrate 31 and merely supported by a support/base substrate 32 via die attach pad 36.[2] According to Jones et al., the support/base substrate is wider than the opening but smaller than the substrate 31 just to form a lower cavity surface and thinner than conductive solder balls before their reflow.[3] Also, the die attach pad 36 is provided merely for attachment of the semiconductor die 18 to the support/base substrate 32 and can be any of epoxy, metal, PCB and ceramic.[4]

Therefore, it is respectfully submitted that the structure recited in Claim 1 is believed to be distinguishable from both Sakamoto et al. and Jones et al., and because Sakamoto et al.

[1] See, for example, Sakamoto et al., column 4, lines 5-9.
[2] See, Jones et al., column 3, lines 5-23.
[3] Id.
[4] See, Jones et al., column 3, lines 31-34.

and Jones et al. fail to disclose the second substrate as recited in amended Claim 1, their teachings even combined do not render the multi-layer printed wiring board recited in Claim 1 obvious.

Londa is cited for the conductive bumps and is not believed to teach or suggest the " second substrate ..., wherein the IC component is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC component" as recited in amended Claim 1. Thus, the structure recited in Claim 1 is also believed to be distinguishable from Londa, and it is believed that its teachings do not remedy the deficiencies of Sakamoto et al. and Jones et al. and render the multi-layer printed wiring board recited in Claim 1 obvious.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 3, 4, 6-8, 11, 12 and 18-20 depend directly or indirectly from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 3, 4, 6-8, 11, 12 and 18-20 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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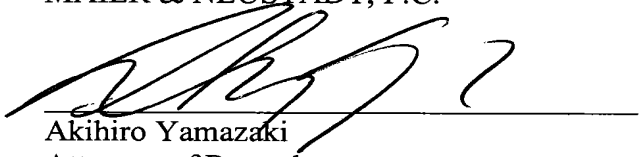

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